

MMBT3906T

MMBT3906T SOT-523 Silicon General Purpose Transistor (PNP)

General description

SOT-523 Silicon General Purpose Transistor (PNP)

FEATURES

- Simplifies Circuit Design
- RoHS Compliant
- Green EMC
- Matte Tin(Sn) Lead Finish
- Weight: approx. 0.002g

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

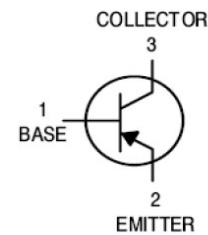
Symbol	Parameter	Value	Units
V_{CB0}	Collector-Base Voltage	-40	V
V_{CE0}	Collector-Emitter Voltage	-40	V
V_{EB0}	Emitter-Base Voltage	-5	V
I_C	Collector Current	-200	mA
P_D	Power Dissipation (FR-4 Board – minimum pad)	200	mW
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient	600	$^\circ\text{C}/\text{W}$
T_J T_{STG}	Junction & Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Green Product

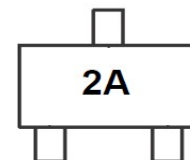


SOT-523 (SC-75A)

Electrical Symbol:



Device Marking :



Off Characteristics

Symbol	Parameter	Test Condition	Limits		Unit
			Min	Max	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 1)	$I_C = -1\text{mA}$, $I_B = 0\text{A}$	-40	-	Volts
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = -10\mu\text{A}$, $I_E = 0\text{A}$	-40	-	Volts
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = -10\mu\text{A}$, $I_B = 0\text{A}$	-5	-	Volts
I_{BL}	Base Cutoff Current	$V_{CE} = -30\text{V}$, $V_{EB} = -3\text{V}$	-	-50	nA
I_{CEX}	Collector Cutoff Current	$V_{CE} = -30\text{V}$, $V_{EB} = -3\text{V}$	-	-50	nA

Note 1: Pulse Test. Pulse width <300us, Duty cycle < 2.0%

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On Characteristics

Symbol	Parameter	Test Condition	Limits		Unit
			Min	Max	
H_{FE}	DC Current Gain	$I_C = -0.1\text{mA}, V_{CE} = -1\text{V}$	60	-	-
		$I_C = -1.0\text{mA}, V_{CE} = -1\text{V}$	80	-	
		$I_C = -10\text{mA}, V_{CE} = -1\text{V}$	100	300	
		$I_C = -50\text{mA}, V_{CE} = -1\text{V}$	60	-	
		$I_C = -100\text{mA}, V_{CE} = -1\text{V}$	30	-	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -10\text{mA}, I_B = -1\text{mA}$	-	0.25	Volts
		$I_C = -50\text{mA}, I_B = -5\text{mA}$	-	0.4	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = -10\text{mA}, I_B = -1\text{mA}$	0.65	0.85	Volts
		$I_C = -50\text{mA}, I_B = -5\text{mA}$	-	0.95	

Small-signal Characteristics

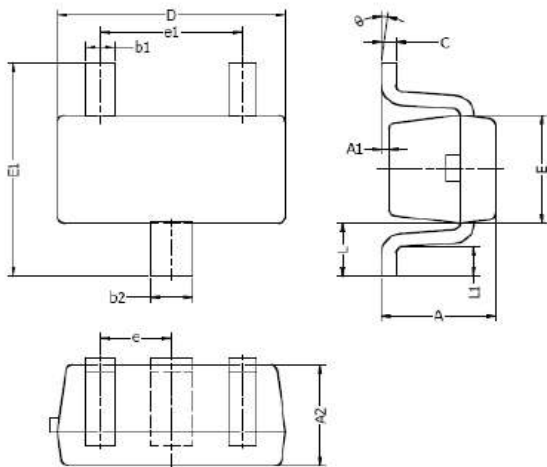
Symbol	Parameter	Test Condition	Limits		Unit
			Min	Max	
f_T	Current-Gain-Bandwidth Product	$I_C = -10\text{mA}, V_{CE} = -20\text{V}, f = 100\text{MHz}$	250	-	MHz
C_{obo}	Output Capacitance	$V_{CB} = -5\text{V}, I_E = 0\text{A}, f = 1.0\text{MHz}$	-	4.5	pF
C_{ibo}	Input Capacitance	$V_{BE} = -0.5\text{V}, I_C = 0\text{A}, f = 1.0\text{MHz}$	-	10	pF
h_{ie}	Input Impedance	$V_{CE} = -10\text{V}, I_C = -1\text{mA}, f = 1.0\text{kHz}$	2	12	pF
h_{re}	Voltage Feedback Ratio	$V_{CE} = -10\text{V}, I_C = -1\text{mA}, f = 1.0\text{kHz}$	0.1	10	$\times 10^{-4}$
h_{fe}	Small-signal Current Gain	$V_{CE} = -10\text{V}, I_C = -1\text{mA}, f = 1.0\text{kHz}$	100	400	-
h_{oe}	Output Admittance	$V_{CE} = -10\text{V}, I_C = -1\text{mA}, f = 1.0\text{kHz}$	3	60	mhos
NF	Noise Figure	$V_{CE} = -5\text{V}, I_C = -100\mu\text{A}$ $R_s = 1.0\text{k}\Omega, f = 1.0\text{kHz}$		4	dB

Switching Characteristics

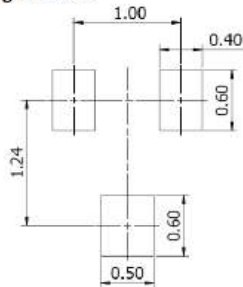
Symbol	Parameter	Test Condition	Limits		Unit
			Min	Max	
t_d	Delay Time	$V_{CC} = -3\text{V}, V_{BE} = -0.5\text{V},$	-	35	nS
t_r	Rise Time	$I_C = -10\text{mA}, I_{B1} = -1\text{mA}$	-	35	
t_s	Storage Time	$V_{CC} = -3\text{V}, I_C = -10\text{mA},$	-	225	nS
t_f	Fall Time	$I_{B1} = I_{B2} = -1\text{mA}$	-	75	

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SOT-523 PACKAGE OUTLINE



Typical Soldering Pattern:



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
A1	0.00	0.10	0.000	0.004
A2	0.70	0.80	0.028	0.031
b1	0.15	0.25	0.006	0.010
b2	0.25	0.35	0.010	0.014
c	0.10	0.20	0.004	0.008
D	1.50	1.70	0.059	0.067
E	0.70	0.90	0.028	0.035
E1	1.45	1.75	0.057	0.069
e	0.50 TYP.		0.020 TYP.	
e1	0.90	1.10	0.035	0.043
L	0.40 REF.		0.016 REF.	
L1	0.10	0.30	0.004	0.012
θ	0°	8°	0°	8°

NOTES:

1. Above package outline conforms to JEITA EAIJ ED-7500A SC-75A.
2. Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

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